



VD SemiX Insights

Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VD SemiX)

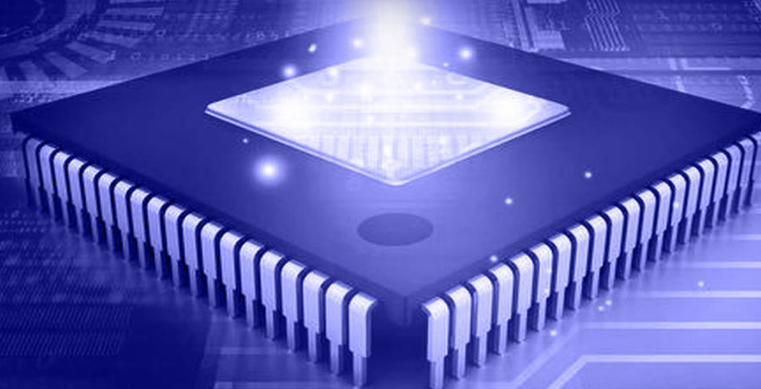
DELHI TECHNOLOGICAL UNIVERSITY



Shri Vinod Dham

Shri Vinod Dham is an Indian-American engineer, entrepreneur, and venture capitalist. He graduated with a BE degree in Electrical Engineering from Delhi College of Engineering in 1971 at the age of 21. He is known as the 'Father of the Pentium Chip' for his contribution to the development of Intel's Pentium micro-processor. In 2025, he was awarded the Padma Bhushan by the Government of India. He is also a mentor and advisor, and sits on the boards of companies, including startups funded through his India-based fund Indo-US Venture Partners, where he is the founding managing director.

Vinod Dham's accomplishments as 'Pentium Engineer' and as an Indian-American technology pioneer from Silicon Valley were observed at an exhibition on South Asians at the National Museum of Natural History, highlighting Indian-Americans who have helped shape America.



VISION OF THE CENTRE



To stimulate and create a robust R & D ecosystem that drives innovation, IP and start-ups in Semiconductor Technology and Microelectronics to cater to the Nation's scientific demands; and serve as a Centre of National and Strategic importance.

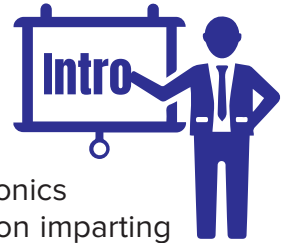
MISSION OF THE CENTRE



- To be a trusted technology and capacity provider of the global Semiconductor and Microelectronics industry with a sustainable impact through innovative semiconductor technologies and solutions.
- To create environment of research, collaboration, innovation and skill development bridging the gap between academia and industry.
- To provide ethics and value-based education by promoting activities addressing the societal needs.
- To enable students develop skills to solve complex technological problems of current times and create world class professionals competent enough in the area of Semiconductors and Microelectronics.

INTRODUCTION

Delhi Technological University has recently established the Vinod Dham Centre of Excellence For Semiconductors and Microelectronics (VDSemiX) in May 2023 with a focus on imparting training & research in thrust areas of Semiconductor Technology and IC Manufacturing; and to provide a platform to boost productivity, address emerging skill gaps and align training & research with industry needs. Thus, in order to support the Government's India Semiconductor Mission and create a skilled manpower for Semiconductor Chips and manufacturing industry, the Centre has been established with a vision to stimulate and create a robust R & D ecosystem that drives innovation, IP and start-ups in Semiconductor Technology and Microelectronics to cater to the Nation's scientific demands; and serve as a Centre of National and Strategic importance.



OBJECTIVES



1. To establish a centralized state of the art infrastructure facility for next generation device design/ materials research/fabrication and sustain educational resources for cutting edge Research and Development in Semiconductor and Microelectronics.
2. Capacity building in terms of skilled manpower at different levels such as technicians, supervisors and engineers in the area of Semiconductor Technology, IC Manufacturing and Microelectronics.
3. Design the curriculum with desired skill sets in research, design, fabrication, equipment manufacturing, packaging, and other related fields for development of Indian semiconductor and display ecosystem.
4. To offer internship opportunities to the students of degree, diploma and certificate level institutions at state and national levels under Govt of NCT of Delhi.
5. To offer M.Tech and Ph.D. programmes in the area of Semiconductors, IC Manufacturing and Microelectronics.
6. Collaboration between Delhi Technological University and Semiconductors/Microelectronics Industry in order to align training & research as per industry needs.



ACADEMIC PROGRAMMES

Minor Specialization in Semiconductors and Microelectronics for B.Tech students

Ph.D. Programme in Semiconductors and Microelectronics

CORE TEAM OF THE CENTRE

DIRECTOR, VDSemiX



Prof. Rishu Chaujar, Fellow of NASI, SERB Power, IETE, OSI

Deptt. of AP

Specialization : Semiconductor Device Modeling & Simulation- Analysis of Novel Device Structures, FinFETs, Nanowire FETs, Tunnel FETs, HEMTs for Biomedical, Wireless & Sensor Applications

Email: chaujar.rishu@dtu.ac.in

ASSOCIATED MEMBERS



Prof. Neeta Pandey

Deptt. of ECE

Specialization : Analog and Digital V.L.S.I Design and Current mode ADC Design

Email: neetapandey@dce.ac.in



Dr. M.S. Mehata

Deptt. of AP

Specialization: Fluorescent spectroscopy, quantum dots, organic leds, thin films

Email: msmehata@dtu.ac.in



Dr. Deva Nand

Deptt. of ECE

Specialization : Analog Integrated Circuits, VLSI Design, Analog Circuit Designing, Low Power Circuit Designing, Digital System Designing using FPGAs

Email: devkamboj@dce.ac.in



Dr. Bharti Singh

Deptt. of AP

Specialization : Thin films and Nano-structures deposition techniques, Resistive Memory Devices, 2D layered materials, synthesis using CVD, Piezoelectricity

Email: bhartisingh@dtu.ac.in



Dr. Mukhtiyar Singh

Deptt. of AP

Specialization: Theoretical Condensed Matter Physics, Density Functional Theory, Topological insulators and low dimensional systems

Email: mukhtiyarsingh@dtu.ac.in



Dr. Sumit Kale

Deptt. of ECE

Specialization : Microelectronics, V.L.S.I Design and Novel Semiconductor Devices

Email: sumitkale785@gmail.com



Mr. Akshay Mann

Deptt. of ECE

Specialization : Microelectronics and Mixed Signal Design

Email: Akshay.mann@dtu.ac.in



Dr. Chaudhry Indra Kumar

Deptt. of EE

Specialization : VLSI Design

Email: indrachaudhry@dtu.ac.in



Ms. Trasha Gupta

Deptt. of AM

Specialization : Machine Learning, Image Processing

Email: trashagupta@dtu.ac.in



DISTINGUISHED PROFESSORS ENGAGED IN THE CENTRE FROM ACADEMIA AND INDUSTRY

Shri Vinod Dham (Padma Bhushan, 2025 and
“Father of Pentium Chip”), USA

Prof. Kaushik Roy from Purdue University, USA

Prof. Jamal Deen from McMaster University,
Canada

ACHIEVEMENTS AND MILESTONES



a) Awards Received

- Prof. Rishu Chaujar has been awarded with The National Academy of Sciences (NASI) Fellow 2024 (Youngest Awardee in 2024).
- Prof. Rishu Chaujar awarded with DST-SERB Power Fellowship
- Prof. Rishu Chaujar and her Ph.D Scholar received the Best Paper Award in 2nd International Conference on Emerging Trends in Information Technology and Engineering (ICETITE-2024) at VIT Vellore, Feb 22-23, 2024.
- Many faculties of the centre have received the DTU Research Excellence Award.
- Many faculties of the centre (Prof. Rishu Chaujar, Prof. Neeta Pandey, Dr. Mohan Singh Mehata) appeared in the top 2% scientists in the world released by Stanford University, USA.
- Dr. Sumit Kale and his PhD scholar received the best paper award in 8th IEEE EDTM Conference held in 3-6 March Hilton Bangalore.

b) Sponsored Research Projects

- DTU has been selected for extending the support of EDA Tools from Cadence, Synopsys, Mentor, Ansys for the next 4-5 years under the Chip to Startup Programme, Ministry of Electronics and Information Technology (MeitY), Govt. of India: Chief Investigator: Prof. Rishu Chaujar and Co-Chief Investigator: Dr. Sumit Kale.

- Prof. Rishu Chaujar awarded with the SERB-Power Research Grant of Rs.38.1 Lacs.
- Dr. Bharti Singh has been awarded SERB-SURE research project Grant of Rs.31.6 Lakhs.
- Dr. Mukhtiyar Singh has been awarded SERB sponsored research project entitled “Machine Learning Assisted First-principles Study of Anomalous Nernst Effect in Weyl Semimetals” worth Rs. 28 Lakhs.
- Dr. Sumit Kale has been awarded SERB sponsored research grant of 29.65 Lakhs.

c) MoUs & Collaborations

- Delhi Technological University signed an MoU with Semiconductor Laboratory (SCL), Chandigarh on 08 November, 2023
- An International MoU from National Chi Nan University in Taiwan has also been received for finalization.
- MoU with SoCTeamup, VLSI Society of India (VSI), Electronics Sector Skills Councils of India (ESSCI) have also been approved.
- Further, collaborations with IESA, SSPL, Applied Materials are already in process.
- The Centre is also in process of having a consortium of institutes/universities such as IIT Delhi, IIT Mandi, IIT Ropar etc. so as to have an exchange of expertise between the universities for future research and skill upgradation. This would maximise the utilization of high end resources available at these places.

d) Patent Granted/Published

- Dr. Mohan Singh Mehata, V. Sharma, A. Tandon – Light-emitting metal and dual metal-doped zinc selenide quantum dots and method thereof – Granted – Patent No: 531913 – Date: 05.04.2024
- Dr. Mohan Singh Mehata – Apparatus and method for detecting electric field modulated absorption and photoluminescence of a sample – Granted – Patent No: 529469 – Date: 21.03.2024
- Dr. Mohan Singh Mehata – System and method for detecting trivalent metal ions – Granted – Patent No: 463021 – Date: 27.10.2023
- Dr. Mohan Singh Mehata, Aneesha – Probe for the detection of ferric ions in aqueous environments and method thereof – Granted – Patent No: 481999 – Date: 13.12.2023
- Prof. Rishu Chaujar, Shivam Gupta – A New Design for an All-Back Contact CIGS Solar Cell – Published – Patent No: 201911027963 – Date: 20.09.2023
- Dr. Chaudhry Indra Kumar, Promit Mandal, Rishabh Sharma- A System and Method for Providing Realtime Availability Of Electric Charging Slots For Vehicles – Published – Patent No: 202311062846 – Date: 21.03.2025
- Prof. Rishu Chaujar and Yash Pathak, “Unveiling the Properties of Ag-Doped SnO₂: A Combined Approach Using Experimental Studies and DFT Calculations” Patent Filed- 2025
- K. Verma and R. Chaujar, “Unveiling the Impact of Interfacial Trap Charges on Strained VS-FeFinFETs for Improved Reliability: Device to Circuit Level Assessment,” *IEEE Transactions on Nanotechnology*, vol. 24, pp. 88-95, 2025.
- K. Verma and R. Chaujar, “Reliability Analysis of the Intricacies of Interfacial Trap Charges in HD-VS-FeFinFET and Its Applicability as CMOS Inverter,” *Microelectronics Reliability*, vol. 166, p. 115610, 2025.
- O. K. Gupta, N. Pandey, and M. Gupta, “Frequency Compensation of Three-Stage Amplifier with Self-Cascode Structure and DT MOS Transistor with Active LHP Zero Circuit,” *Journal of Circuits, Systems and Computers*, 2025.
- L. Soni and N. Pandey, “A Robust, Low Power and High-Speed Radiation Hardened 12T SRAM Cell for Space Applications,” *Microelectronics Journal*, vol. 156, p. 106502, 2025.
- Aneesha and M. S. Mehata, “Waterborne Explosives: A Rapid Detection Method Using MoSe₂ Quantum Dots,” *Materials Research Bulletin*, vol. 185, p. 113287, 2025.
- S. Kaul, S. Yadav, S. Rewari, and D. Nand, “Analytical Modelling of Temperature Resilient Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor,” *IEEE Transactions on Dielectrics and Electrical Insulation*, 2025.
- N. Sharma, U. K. Dwivedi, U. T. Nakate, M. Singh, and S. P. Choudhury, “Gas-Sensing Properties of NO on Ce-Doped Zinc Oxide: A DFT Study,” *Particle & Particle Systems Characterization*, vol. 42, no. 1, p. 2400126, 2025.
- R. Kumar and M. Singh, “Appearance of Topological Phase in YAs Semimetal Under Hydrostatic Pressure and Epitaxial Strain,” *Journal of Physics and Chemistry of Solids*, vol. 196, p. 112356, 2025.

e) Research Publications

IN 2025

- S. Sharma, J. Madan, and R. Chaujar, “Insights Into Temperature Sensitivity Analysis of Polarity Controlled Charge Plasma Based Tunable Arsenide/Antimonide Tunneling Interfaced Junctionless TFET,” *IEEE Transactions on Nanotechnology*, vol. 24, pp. 96-101, 2025.

- R. Kumar, R. Kumar, A. Sihi, and M. Singh, "Unraveling the Topological Phase in Zintl Semiconductors $RbZn_4X_3$ ($X = P, As$) Through Band Engineering," *Journal of Physics: Condensed Matter*, 2025.
- S. Rana et al., "PVDF/N-rGO Nanofibers Based Sustainable Triboelectric Nanogenerator for Self-Powered Wireless Motion Sensor," *Carbon*, vol. 234, p. 119926, 2025.
- S. R. R. Upadhyay, S. Kale, and A. Pandey, "Dielectric Modulated InAs Pocket Heterojunction Tunnel FET for Biosensor Applications," *ECS Journal of Solid State Science and Technology*, 2025.

IN 2024

- R. Mann and R. Chaujar, "DFT-Based Atomic Calculation of Si-Doped HfO_2 and Effect of Its Negative Capacitance on Analog/RF, and VTC Parameters of MOSFET," *Silicon*, vol. 16, pp. 1237–1252, 2024.
- Anshul and R. Chaujar, "Semi-Empirical DFT Based Investigation of Electronic and Quantum Transport Properties of Novel GS-AGNR (N) FET," *IEEE Transactions on Nanotechnology*, vol. 23, pp. 400-407, 2024.
- O. K. Gupta, N. Pandey, and M. Gupta, "Improved Frequency Compensation Technique of Three-Stage Amplifier Using Class AB Flipped Voltage Follower and Slew Rate Enhancer Circuit," *AEU - International Journal of Electronics and Communications*, vol. 177, p. 155173, 2024.
- L. Soni and N. Pandey, "A Single Bitline Highly Stable, Low Power With High Speed Half-Select Disturb Free 1T1R SRAM Cell," *ACM Transactions on Design Automation of Electronic Systems*, vol. 29, 2024.
- L. Soni and N. Pandey, "A Reliable and High-Performance Radiation Hardened Schmitt Trigger 1T1R SRAM Cell for Space Applications," *AEU - International Journal of Electronics and Communications*, vol. 176, p. 155161, 2024.
- Isha, M. S. Mehata, and Mohan Singh, "Synthesis of Graphene Quantum Dots (GQDs) from Paddy Straw for Bilirubin Detection," *Plasmonics*, vol. 20, pp. 2359-2366, 2024.
- S. Husain et al., "Quantum Computational and Spectroscopic Investigation of 3-Aminosalicylic Acid," *Journal of Fluorescence*, 2024.
- S. Kumari, D. Nand, and S. Kant, "MOS-Based Electronically Tunable Current-Mode Dual-Output Full-Wave Rectifier Using Single DDCCTA," *Electrical Engineering*, 2024.
- S. Kumari and D. Nand, "Simplified Wave Active Filter: A Novel Design in Current Mode with Single EX-CCCCTA," *Journal of Circuits, Systems and Computers*, vol. 34, 2024.
- S. Kaul et al., "Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) for Improved Performance and Off-State Leakage Reduction," *ECS Journal of Solid State Science and Technology*, vol. 13, no. 10, 2024.
- P. Yadav et al., "Performance Enhancement of a Hybrid Solar Still/Photovoltaic System with Mirror Reflectors, Automatic Water Cooling, and Feed Water Preheating," *Russian Physics Journal*, vol. 67, pp. 62–69, 2024.
- V. Singh et al., "Electrospun PVDF-MoSe₂ Nanofibers Based Hybrid Triboelectric Nanogenerator for Self-Powered Water Splitting System," *Journal of Alloys and Compounds*, vol. 978, p. 173416, 2024.
- K. Sharma, N. K. Puri, and B. Singh, "An Efficient Electrochemical Nano-Biosensor Based on Hydrothermally Engineered Ultrathin Nanostructures of Hexagonal Boron Nitride Nanosheets for Label-Free Detection of Carcinoembryonic Antigen," *Applied Nanoscience*, vol. 14, pp. 217–230, 2024.
- K. Komal, M. Singh, and B. Singh, "A Flexible Memory Device Made of SnO₂-hBN Nanocomposite Exhibits Stable Resistive Switching Application," *Journal of Materials Science*, vol. 59, pp. 13508–

13531, 2024.

- R. Kumar, M. Singh, and A. Vij, "Unraveling the Effect of Pressure on Structural Phase Transition, Electronic, and Optical Properties of $\text{Hf}_{1-x}\text{Si}_x\text{O}_2$ ($x= 0, 0.03, 0.06, 0.09$): A First-Principles Investigation," *Journal of Physics and Chemistry of Solids*, vol. 185, p. 111773, 2024.
- R. Kumar, R. K. Bibiyan, and M. Singh, "Emergence of Topological Phase and Non-Trivial Surface States in Rare-Earth Semimetal GdSb with Pressure," *Journal of Physics D: Applied Physics*, vol. 58, no. 1, p. 015304, 2024.
- T. Gupta, R. K. Agrawal, R. Sangal, and S. Avinash Rao. "Performance Evaluation of Thermography-Based Computer-Aided Diagnostic Systems for Detecting Breast Cancer: An Empirical Study." *ACM Transactions on Computing for Healthcare*, vol. 5, no. 4, pp. 1-30, 2024.
- T. Gupta, I. Sreedevi, and R. Jindal. "Segmenting hotspots from medical thermal images using Density-based modified FC-Pc FS with spatial information." In *Quantitative InfraRed Thermography Journal* pp. 1-37, 2024.
- Kumar, A. Chaudhary, and S. Upadhyaya. "Design of high performance energy efficient CMOS voltage level shifter for mixed signal circuits applications." *Integration* vol. 95 pp. 102133, 2024
- V.Thakur,A.Kumar,andS.Kale. "Numerical modeling and performance analysis of underlap gate cavity-integrated reconfigurable silicon nanowire Schottky barrier transistor biosensors." *Applied Physics A* vol. 130, no. 11, pp 1-13, 2024
- T. Garg, and S. Kale. "Recent Developments, Reliability Issues, Challenges and Applications of GaN HEMT Technology." *IEEE Electron Devices Reviews*, 2024.
- Kumar, and S. Kale. "Noise and sensitivity analysis of the dielectric modulated reconfigurable SiNW-SBT for biosensor applications." *Micro and Nanostructures* 193 (2024): 207923.
- Mann, N. Pandey, and M. Gupta. "Novel high speed low power comparators imbibing Self-cascode preamplifier technique." *AEU-International Journal of Electronics and Communications* 185 (2024): 155429.

f) Students Society

- Semicon Society has been introduced under the Centre and its main agenda is organizing events, workshops, seminars, conferences etc. centred on semiconductors and microelectronics, to build awareness of semiconductor career paths, sessions related to the chip industry and including the buzzword of semiconductors.

SEMIX Library – A Hub for Microelectronics and Semiconductor Knowledge

The SEMIX Library, established within the Vinod Dham Center of Excellence for Semiconductor and Microelectronics, serves as a dedicated space for fostering awareness and advancing knowledge in the field of Semiconductor and Microelectronics. This specialized library houses an extensive collection of books covering diverse topics such as semiconductor device physics, analog and digital circuit design, ASIC and SoC design, embedded systems, compact modeling of semiconductor devices, solid-state memories, digital signal processing,

chiplet design, and VLSI technology. The collection features work by both renowned Indian and international authors, ensuring access to the latest advancements and research in the field. Beyond just a repository of knowledge, SEMIX Library provides an intellectual space for innovation, encouraging new ideas and supporting cutting-edge research in microelectronics. By offering valuable resources to students, researchers, and Faculties, it plays a crucial role in driving advancements in semiconductor technology.

RELATED INFRASTRUCTURE

Equipment and measurement instrument



Thermal Evaporation HHV Smart Coat 3.0



Oven



Mixed Domain Oscilloscope 3 Series



Keithley Sourcemeter 2450



Furnace MF-12P(A)



Digital Multimeter DMM7510

Integrated Electronics
Design Automation
(EDA) Tools for Chip
Design

ATLAS
SILVACO

cadence
Virtuoso

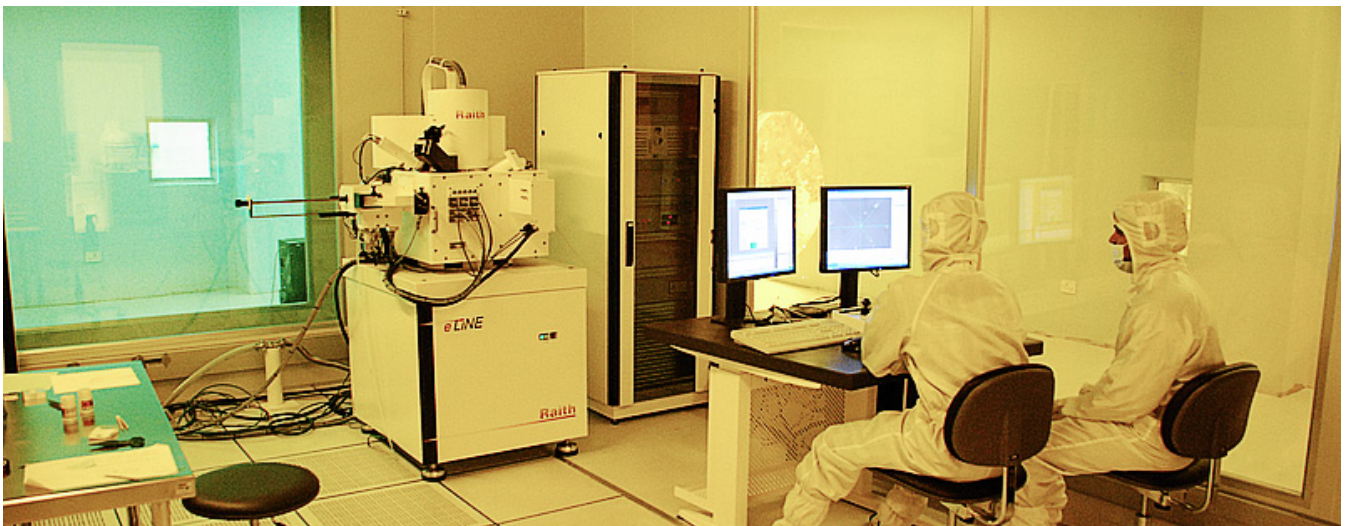
Visual
TCAD

XILINX.

Sentaurus

QuantumATK

Upcoming Class 1000 Clean Room Facility





Events Organized under the Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDSemiX)

1. One Day Workshop on Atomistic Modeling using Synopsys Quantum ATK for Nanomaterials/ Nano Devices held on January 11, 2024 in Pragyan Hall, DTU.

Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDCoE4SM) DELHI TECHNOLOGICAL UNIVERSITY

Organizes
One Day Workshop
on
Atomistic Modelling using Synopsys Quantum ATK for Nanomaterials / Nano Devices

TOPICS TO BE COVERED

- Introduction to Quantum ATK Software
- Types of Simulators in Quantum ATK
- General Work-Flow In Quantum ATK
- Density Functional Theory (DFT)
- Non-Equilibrium Green Function (NEGF)
- Advanced Calculation and Analysis
- Material Building Library
- Optimization of Geometry
- Scripting In Quantum ATK
- Live Demonstration of Quantum ATK
- Virtual Nano Lab (VNL)
- Nano-Structured Materials and Devices
- Atomistic Modelling
- Bulk/Molecule Configuration
- Doping and Spatial Region for Devices

11th JANUARY, 2024
11:00 AM - 4:00 PM
PRAGYAN HALL, DTU

Please Register at URL:
<https://forms.gle/Ka3fWyt5rr44uy0Y6>

INTEGRATED MICROSYSTEM
Design. Prototype. Scale.

SYNOPSYS
QUANTUMATK

Scan for Registration

Mr. Ayush Singh
(Application Engineer)
+91-7703690784
ayush@ims-india.org

CHIEF PATRON
Prof. Prateek Sharma
Hon'ble Vice Chancellor

PATRON
Prof. Madhusudan Singh
Registrar

CHAIRPERSON
Prof. Rishu Chaujar
Centre Coordinator-VDCoE4SM

CONVENORS
Dr. Deva Nand
Dr. Mohan S. Mehata



2. An Academic Interaction with Dr. Satya Gupta, President VLSI Society Of India on the Theme: Semiconductors held on January 18, 2024 in Conference Hall, Science Block, DTU.



Vinod Dham Centre of Excellence for Semiconductors and Microelectronics DELHI TECHNOLOGICAL UNIVERSITY

Organizes
An Academic Interaction
with
Dr. Satya Gupta
President, VLSI Society of India

THEME : Semiconductors

- Interaction with Faculty.
- Interaction with Students.
- Possible collaboration with VLSI Society of India & Vinod Dham Centre of Excellence for Semiconductors & Microelectronics for creation of industry, academia & government connect across the areas of:
 - a. Design and Research.
 - b. Talent, Skilling & Startups.

CHIEF PATRON
Prof. Prateek Sharma
Hon'ble Vice Chancellor

PATRON
Prof. Madhusudan Singh
Registrar

CHAIRPERSON
Prof. Rishu Chaujar
Centre Coordinator - VDCoE4SM

CONVENOR
Mr. Akshay Mann
Member- VDCoE4SM

18th JANUARY, 2024 **11:00 AM Onwards**

Conference Hall, First Floor, Science Block, DTU

3. An Industrial Interaction with Mr. MG Hwang-VP and GM, Silvaco, Asia and Mr. Zhao Qingda, MD, Silvaco, Singapore held on January 23, 2024 in Conference Hall, Science Block, DTU.

Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDCoE4SM)
DELHI TECHNOLOGICAL UNIVERSITY

Organizes
An Industrial Interaction
with
Mr. M G Hwang (VP & GM, Silvaco, Asia) and **Mr. Zhao Qingda** (MD, Silvaco, Singapore)

Key Highlights :

- Interaction with Faculties.
- MoU between Vinod Dham Centre of Excellence for Semiconductors & Microelectronics & Silvaco.
- Collaboration in Teaching, Research & Development.
- Cooperation in Projects, Research & Consultancy Activities.
- Exchange of Students for Summer/Winter Internships.
- Publication of Intellectual Properties (IPs).
- Cooperation in Curriculum Development.

CHIEF PATRON
Prof. Prateek Sharma
Hon'ble Vice Chancellor

PATRON
Prof. Madhusudan Singh
Registrar

CHAIRPERSON
Prof. Rishu Chaujar
Centre Coordinator VDCoE4SM

23rd January 2024 11:00 AM
Conference Hall, First Floor, Science Block, DTU



4. Live Streaming of India's Techade-Chips for Viksit Bharat -Address of Hon'ble PM on 13th March, 2024

In pursuit of the vision of the Viksit Bharat, the Hon'ble Prime Minister laid foundation stone for setting up of three semiconductor facilities at the following places:

- TEPL, India's first fab facility in Dholera, Gujarat;
- TEPL OSAT facility in Morigaon, Assam and
- CG Power OSAT facility in Sanand, Gujarat.

Students and Faculties are key stakeholder of this endeavour; therefore, all the departments were requested to ensure that all students, especially of STEM and technical disciplines participate in above programme. The programme was started at 9.30 AM on 13th March, 2024 at Committee Room, Science Block-1st Floor where there was live streaming of address of Hon'ble Prime Minister at 10.30 AM. The posters related to the event is attached.

India's Techade

CHIPS FOR VIKSIT BHARAT

Laying of Foundation Stone of 3 Semiconductor Facilities

13th March, 2024, Wednesday
Programme Starts: 9:30 AM
Hon'ble PM's Address: 10:30 AM

Address of PM to the Youth
across the country on the occasion

Watch Live /@NarendraModi

5. A 2-day International Conference on Microelectronics, Circuits and Systems-MICRO 2024 on May 16-17, 2024 in association with Applied Computer Technology, Kolkatta. Supported by IEEE EDS Delhi Chapter and Applied Materials Pvt.Ltd.



**11th International Conference
on
MICROELECTRONICS, CIRCUITS AND SYSTEMS (MICRO 2024)**
16th-17th MAY, 2024

Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDCoE4SM)
Delhi Technological University, Bawana Road, Shahbad Daulatpur, Rohini, Delhi-110042, India
in collaboration with Applied Computer Technology, Kolkata, West Bengal, India

HYBRID CONFERENCE Website: www.actsoft.org/micro2024 | Email: micro2024@dtu.ac.in

TOPICS OF INTEREST

- Nano-structures and Nanomaterials
- Photolithography and Nanofabrication
- Silicon and III-V Technology, CMOS scaling Issues
- Sensors, Actuators & Transducers
- Analog RF and digital Circuits, Power Electronics
- Photonic, Solid-state lighting, Silicon and III-V Photonics
- Hybrid of soft computing and statistical learning techniques
- Biomedical Electronics, MEMS and NEMS
- Nano devices, VLSI system, circuit and design
- Image Sensing and Processing, Wireless Communication
- Memory Devices: SRAM, DRAM, PRAM, Micro-lens, Micro-mirror
- Coding and security of systems, Modelling and Simulation
- Fault Detection, Isolation and Recovery
- Optical fibre and communication
- Main-Machine Interface Design
- Real Time Embedded System
- Speech recognition in Robotic system
- Microstrip Antennas and Diversity
- IoT and industry-4
- Micro Mechatronics
- Signal Processing
- Machine Learning
- Off-shore Energy Systems
- Pattern Formation
- Photovoltaics
- Plasma Physics and Engineering
- Virtual Laboratory

CALL FOR PAPERS

Introduction of Micro2024
It is a series of annual conference, 11th version of Micro2024 will be organized in Delhi, the Capital City of India. We accept good papers for presentations in this conference. Papers should be unpublished and original research works with results and new findings. Some good papers as tutorials-on any theme of the conference, survey papers etc. may be presented in this conference. This conference was born with high quality publications and in every years, we publish some good extended versions of papers in the Special Issue of the Journal of Microsystem Technologies of Springer-Nature, SCI indexed having Impact Factor=2.1 and Q2/Q3 ranked. Also, we have published many Proceedings of LNEE (Lecture Notes in Electrical Engineering), Springer-Nature, SCOPUS indexed, Impact Factor=0.5 with some other papers of this conference.

Proposed Publications
This conference deals with best quality research papers. Abstracts or partial papers are not considered in this conference. After presentation to the conference and after completion of the conference, one month time is given to the authors for preparing extended version of the paper.

- For Micro2024, we have a plan to publish a Special Issue of the Journal of Microsystem Technologies, SCI indexed, Impact Factor=2.1, Springer-Nature, with some good papers of this conference.
- It is planned to publish the peer reviewed and some selected and good papers of this conference as a proceeding of LNEE Book series of Springer-nature, Scopus indexed, <https://www.springer.com/series/7818> For detailed instructions for author and editors of conference proceedings, kindly visit the following link: <https://www.springer.com/us/authors-editors/conference-proceedings>

Flow of Paper Submission

- Login to : <https://cm3.research.microsoft.com/micro2024>
- login with existing email/ password or create a new account
- Note down the paper ID which will be used for next all communications.
- After some days, we shall send Paper acceptance notice to you from cm3@Microsoft.com
- If accepted, do registration by paying Fee to our Company's Bank Account.
- Present paper in the conference venue as offline/online.
- After the conference, we shall send email to you about publication of your paper.

For registration and registration fee, please visit the Website: www.actsoft.org/micro2024
Submission Deadline for Full-Length Paper: **April 15, 2024**

6. Industrial Visit: Solid State Physics Laboratory (SSPL), DRDO

Students of the Applied Physics; and Electronics and Communication Engineering departments visited SSPL Delhi on 4th October 2024 with the purpose of an industrial visit accompanied by Prof. Rishu Chaujar (Applied Physics department) and Dr. Deva Nand (Electronics and Communication Engineering department).



Solid State Physics Laboratory, a premier DRDO semiconductor research laboratory, was established in 1962 with the broad objective of developing an R&D base in the field of Solid-State Materials, Devices, and sub-systems. Ever since SSPL has worked relentlessly to achieve distinction in the Indigenous development of semiconductor materials and devices.

Students visited the laboratories which were equipped with advanced facilities for Nano-fabrication, Crystal growth and epitaxy, including Electron Beam Lithography, Focused Ion Beam, III-As/N/Sb & II-VI MBEs, III-N/As MOCVDs etc. All the students were divided into two groups and sent for the visit of SiC (Silicon Carbide) wafer and GaAs (Gallium Arsenide) crystal growth sub-laboratories of the SSPL. In addition to lab visits, products and achievements of SSPL DRDO were also shown to the students via a video lecture. The visit was very successful and it was a good learning experience for the students.

The centre has also organized one week ATAL sponsored Faculty Development Programme on “Recent Trends in Semiconductor Technology and Chip Design” from 2-7 December 2024.



ABOUT THE INSTITUTE

Delhi Technological University (formerly known as Delhi College of Engineering) located in Delhi is a premier institution of Engineering and Technology in India. The university plays a key role in the national and global knowledge network, empowering India with the wings of knowledge and innovation. The university aims to imbibe a culture of methodical research and to develop a scientific temper for the integration of science, engineering, and management. DTU has been ranked amongst the top institutions in multiple reputed national and international surveys.

ABOUT THE DEPARTMENT

Delhi Technological University has recently established the Vinod Dham Centre of Excellence For Semiconductors and Microelectronics (VDCoE4SM) in May 2023 with a focus on imparting training & research in thrust areas of Semiconductor Technology and IC Manufacturing; and to provide a platform to boost productivity, address emerging skill gaps and align training & research with industry needs. Thus, in order to support the Government's India Semiconductor Mission and create a skilled manpower for Semiconductor Chips and manufacturing industry, the Centre has been established with a vision to stimulate and create a robust R & D ecosystem that drives innovation, IP and start-ups in Semiconductor Technology and Microelectronics to cater to the Nation's scientific demands; and serve as a Centre of National and Strategic importance.

OBJECTIVE OF THE FDP

Semiconductor Technology and modern chip design play a vital role in developing various electronic devices ranging from smartphones and computers to medical

equipment, sensors and, automotive systems, etc. Design, and development of Modern ICs need the knowledge and skills in the rapidly evolving field of circuit design, semiconductor design, and manufacturing. This FDP would likely provide faculty members, research scholars, and postgraduate students deep insight into the latest trends, advancements, and challenges related to emerging nanoscale semiconductor devices, advanced semiconductor sensors, and cutting-edge IC design technology and methodologies. In addition, this program aims to equip the participants with hands-on experience in the state-of-the-art tools for the design, analysis, and investigation of high-performance nanoscale semiconductor devices and circuits, which support analog and digital IC design.

OUTCOME OF THE FDP

FDP plays a crucial role by helping the India Semiconductor Mission (ISM) to educate and foster workforce development in semiconductor design, fabrication, sensors design, and modern IC design. FDP empowers participants with the latest knowledge, design tools, and techniques in these fields. FDP also opens up the path for research opportunities, professional networking with peers, and institutional growth. Hands-on or practical sessions equip participants with new skills and expertise in nanoscale semiconductor devices, sensor technology, and IC design. Also, the interactions between participants with industry experts and research scientists provide deep insight into real-world applications, challenges, and opportunities. This FDP also supported initiatives of the Government of India such as Make in India, Atmanirbhar Bharat, Skill India, Startup India, Digital India, and Vikshit Bharat.

ONE WEEK FACULTY DEVELOPMENT PROGRAM

on

“Recent Trends in Semiconductor Technology and Chip Design”

Dec 2-7, 2024

Organized by



Vinod Dham Center of Excellence for Semiconductors and Microelectronics
Delhi Technological University
Delhi-110042



Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDSemiX)

DELHI TECHNOLOGICAL UNIVERSITY

Bawana Road, Shahbad Daulatpur, Rohini,
Delhi-110042, India

Contact Email: vdcoe4sm@dtu.ac.in